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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,856	10/19/2001	Yasumasa Kasuya	10921.102US01	1107

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,856	KASUYA, YASUMASA	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 08/11/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Upon further consideration of the claim language, the indication of allowable subject matter of claims 7-10 is hereby withdrawn. A full explanation is provided herein below. Any inconvenience is sincerely regretted.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,281,568 to Glenn et al.

Regarding claim 1, Glenn et al. (figs. 2-7) teach a semiconductor device comprising:

a die pad (22) including a first surface (23) and a second surface (24) opposite to the first surface, the second surface (24) including an exposed portion and a retreated portion (a portion of the die pad formed by surfaces [25,26,27]) around the exposed portion (column 5, lines 14-27). It is believed that the reference numeral for the third surface is "25" instead of "24" in column 5, line 25;

a semiconductor chip (52) mounted on the first surface (23) of the die pad (22); and

a sealing resin (51) covering the die pad (22) and the semiconductor chip (52), the resin allowing the exposed portion to be exposed and being held in contact with the retreated portion,

wherein the die pad (22) is formed with at least one slit (a portion of an opening forms between the portion of [22] and [33]) that is open in the retreated portion of the second surface (24) and in the first surface (23).

Regarding claim 4, Glenn et al. teach the die pad (22) is formed with a plurality of silts (the portions of opening form between the portion of [22] and [33]) that are open in the retreated surface of the second surface (24) and in the first surface (23), the plurality of slits being arranged to surround the semiconductor chip (52) (figure 2).

Regarding claim 6, Glenn et al. teach a terminal (a left terminal portion having surfaces [31,32,33]) electrically connected to the semiconductor chip (52) via a wire (54), the terminal being retained by the sealing resin so as to be partially exposed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,281,568 to Glenn et al. in view of US Patent No. 5,410,182 to Kurafuchi et al.

Regarding claim 2, the disclosures of Glenn et al. are discussed as applied to claims 1, 4 and 6 above.

Glenn et al. differ from the claimed invention by not showing the retreated portion is defined by a retreated surface and a side surface which adjoins the exposed portion and forms an acute angle together with the retreated surface. However, Kurafuchi et al. teach the die pad (11), which has an acute angle (column 4, lines 12-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kurafuchi et al. into the device taught by Glenn et al. because it improves the adhesion between the die pad and the sealing resin.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,281,568 to Glenn et al. in view of US Patent No. 6,566,168 to Gang, and further in view of US Patent No. 5,986,333 to Nakamura.

Regarding claim 5, the disclosures of Glenn et al. are discussed as applied to claims 1, 4 and 6 above.

Glenn et al. differ from the claimed invention by not showing the die pad being electrically connected to the semiconductor chip via a wire. However, Gang (figure 7) teaches the die pad (50) being electrically connected to the semiconductor chip (44) via a wire (42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Gang into the device taught by Glenn et al. because it provides interconnection between the chip and the die pad.

Glenn et al. and Gang differ from the claimed invention by not showing the die pad has opening. However, Nakamura (figure 6) teaches the die pad (32) has opening (38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was

made to incorporate the teaching of Nakamura into the device taught by Glenn et al. and Gang because it provides the basis of the automatic recognition of the lead. The combined device shows the semiconductor chip is electrically connected to the die pad via a first wire, the first wire being connected to the first surface of the die pad at a portion between a peripheral edge of the die pad and the at least one slit.

6. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,281,568 to Glenn et al. in view of US Patent No. 6,566,168 to Gang.

Regarding claim 7, Glenn et al. (figures 2-7) teach a semiconductor device comprising a semiconductor chip (52); a die pad (22) including an upper surface on which the semiconductor chip (52) is mounted and a lower surface opposite to the first surface; a plurality of leads (30) electrically connected to the semiconductor chip (52) via wires (54); and a sealing resin (51) enclosing the semiconductor chip (52) in a manner such that the lower surface of the die pad (22) is exposed;

wherein the die pad (22) includes a thin-walled portion formed by removing a part of the lower surface (a portion of the die pad formed by surface [25, 26, 27]) along a peripheral edge of the die pad (22), the die pad (22) formed with at least one slit (a portion of an opening forms between the portion of [22] and [33]) extending through the thin-walled portion.

Glenn et al. differ from the claimed invention by not showing the die pad being electrically connected to the semiconductor chip via a wire. However, Gang (figure 7) teaches the die pad (50) being electrically connected to the semiconductor chip (44) via a wire (42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to incorporate the teaching of Gang into the device taught by Glenn et al. because it provides interconnection between the chip and the die pad. The combined device shows the die pad being electrically connected to the semiconductor chip via a wire.

Regarding claim 8, Glenn et al. teach the sealing resin (51) extends under the thin-walled portion so as not to expose an opening of the slit.

Regarding claim 9, Glenn et al. teach the at least one slit (a portion of an opening forms between the portion of [22] and [33]) extends along at least one side surface of the semiconductor chip (52) around the semiconductor chip (figure 2).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. in view of Gang, and further in view of US Patent No. 5,986,333 to Nakamura.

Regarding claim 10, the disclosures of Glenn et al. and Gang are discussed as applied to claims 7-9 above.

Glenn et al. and Gang differ from the claimed invention by not showing the die pad has opening. However, Nakamura (figure 6) teaches the die pad (32) has opening (38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakamura into the device taught by Glenn et al. and Gang because it provides the basis of the automatic recognition of the lead. The combined device shows the first wire is connected at one end thereof to the semiconductor chip and connected at another end thereof to the die pad at a portion between a peripheral edge of the die pad and the at least one slit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
October 24, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800